tiometer inserted between the two R resistors and connecting the wiper to the –A1 input can reduce the gain error. This adjustment can achieve an error of less than 0.1% before temperature coefficients introduce diminishing returns.

Voltage compliance for a current source defines the range of voltage over which its load can vary without disturbing linear operation. With common-mode and supply-rejection ratios around 100,000 for the OPA2111 dual op amp, and a line regulation of 50 μV/V for the reference, the circuit develops an output resistance of 12,500 × R_S, or 31 MΩ. The result is a negligible 0.032-ppm output error for a full-scale output-current transition. Also, with the 2.5-V reference and the two OPA2111 amplifiers, normal operation is retained to within 6.5 V of the power-supply rail levels.□

CIRCLE 522

REDUCE NOISE IN VOLTAGE REGULATORS

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Simply placing capacitors across the output and the adjust pins of three-terminal regulators is the usual approach to reducing regulator noise. On most regulators, though, the noise voltage over some narrow frequency ranges can peak—even though for typical values of output bypass capacitances, the overall noise voltage over a broad frequency range may drop. Also, the regulator's transient response can experience unexpected effects.

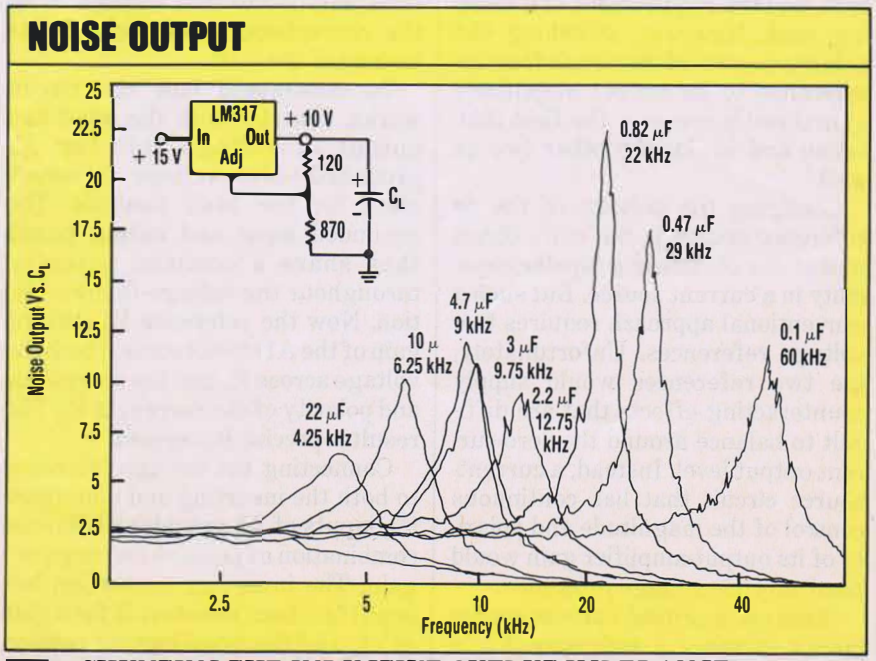
The output impedance of the LM317 voltage regulator, for example, over a 1-kHz to 1-MHz range, is inductive. This is not because of lead inductance, but rather because its internal gain roll-off is 6 dB/octave—just as for an op amp. This characteristic is typically unimportant to average users of IC regulator circuits. But when users shunt this inductive output impedance to ground with a capacitor, the combination can produce a noise peak at the resonant frequency of this inductance and added capacitance *(Fig. 1)*.

For an LM317 with various capacitive loads, the frequency range of the noise spike doesn't extend much above 100 kHz nor below 10 kHz. This is because of ohmic losses in the inductance of the regulator and in the added output capacitance. The frequency is predictable from $1/2\pi\sqrt{LC}$. This information can be scaled and also applied to all other three-terminal voltage regulators.

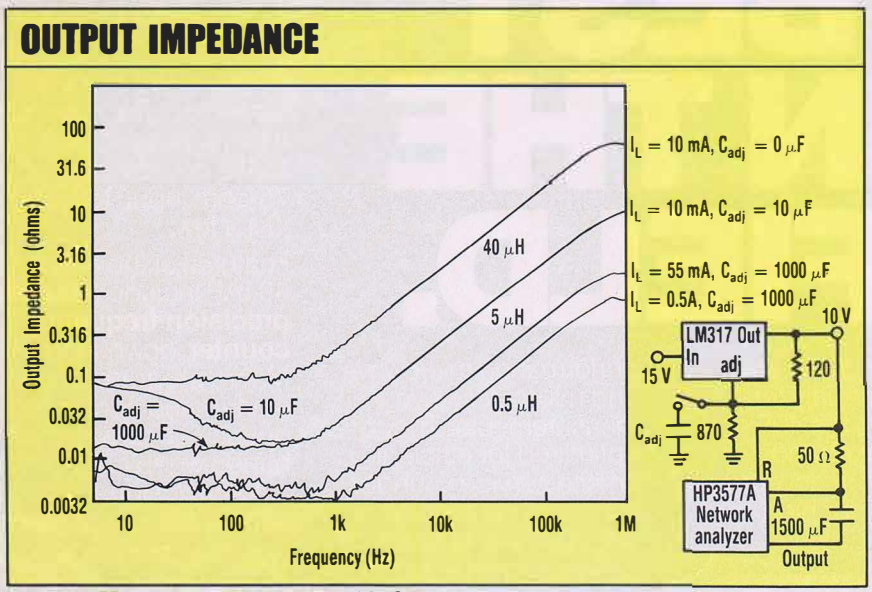
A noise spike's magnitude depends on the Q of the resonant circuit, which the series resistance of the output capacitor mainly dominates. For instance, a good 1-μF polypropylene capacitor with an equivalent series resistance (ESR) of 20 mΩ at 30 kHz produces a noise peak three times greater than that of the same value of tantalum capacitor with an ESR of 1 to 2 Ω. The noise peak also reflects back to the input of the regulator at about 20-dB down from the output.

A little known fact is that the output impedance of three-terminal regulators varies substantially with load current and the programmed output voltage. As load current increases, the transconductance of the regulator's output transistor also increases. This behavior, in turn, causes the output inductance to decrease until the current-limit, bondwire, and lead resistances dominate the output impedance *(Fig. 2)*. Consequently, although many designers have assumed that output impedance versus frequency was one curve, it's actually a family of curves—one for each current level. This phenomenon occurs in both positive and negative regulator types (LM117 and LM137), in adjustable and fixed types (LM140 and LM120), and in high- and low-current regulators (LM138 and LM317LZ).

Fortunately, in most cases, several microvolts of power-supply noise peaking at 5 or 10 kHz won't cause problems. But if the application cir-



1. SHUNTING THE INDUCTIVE OUTPUT IMPEDANCE of a three-terminal regulator to ground with a capacitor can produce a noise peak at the resonant frequency of this inductance and added capacitance.



2. THE OUTPUT IMPEDANCE of three-terminal regulators versus frequency forms a family of curves, one for each current level, which changes the output inductance.

cuit is extremely sensitive to excess noise from the supply at a particular frequency, then users can easily engineer the regulator's circuit so that the noise peak falls outside the critical range. Capacitors between 0.1 to 20 μF, especially those with low ESR, should be avoided in low-noise applications. The most effective noise reduction occurs with electrolytic capacitor sizes of 50 μF or greater connected across the output and at least 1 μF connected from the adjust pin to ground.□

CIRCLE **523**

LOW DISTORTION VIDEO BUFFER

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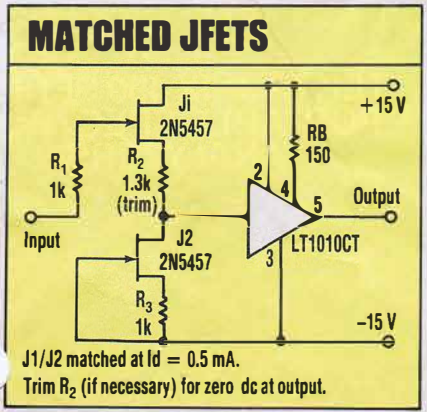

THIS LINEAR buffer amplifier's overall harmonic distortion is a low 0.01% or less at 3-Vrms output into a 500-Ω load with no overall feedback.

Wideband, unity-gain buffers are utilitarian elements for a broad spectrum of circuits, from dc to video frequencies. To execute a buffer, designers can use various approaches, employing one IC or a complex multitransistor discrete circuit. Of course, designers must typically trade-off in one or more areas, such as in dc offset, speed, linearity, and many other circuit parameters. Nevertheless, a buffer circuit using an LT1010CT video amplifier offers an interesting combination of high performance and relative simplicity.

The amplifier offers a 100-V/μs slew rate, a 20-MHz video bandwidth, and 100 mA of output. It has internal short-circuit protection and is relatively easy to use. For especially high-linearity applications, the amplifier can extend class-A operation by using a fifth biasing terminal. In Sallen-Key unity-gain types of active-filter, or even just for general audio use, this extended linearity can be very important.

One accommodation that designers must make, though, is to cancel the LT1010's nominal dc offset of approximately 60 mV. Also, its input impedance needs boosting. Accordingly, the LT1010 is primarily an inside-the-loop op-amp—not a pure standalone unity-gain buffer. Such accommodations make it possible to exploit the device's high output-drive and linearity virtues, and have a circuit with very high input impedance, low bias current, and low dc offset voltage.

In the circuit, a pair of JFETs, J1 and J2, are preselected for a nominal match at the bias level of the linearized source-follower input stage, at about 0.5 mA *(see the figure)*. The source-bias resistor, R_2, of J1 is somewhat larger than R_3 so that it can drop a larger voltage and cancel the LT1010CT's offset. In use, J1 and J2 provide an untrimmed dc offset of ±50 mV or less. Then swapping J1 and J2 or trimming the R_2 value can give a finer match. If resistors R_2 and R_3 were equal, as in the case of classic form of a zero-offset FET buffer, the LT1010CT's offset in the second-stage would still appear at the circuit's output.

The circuit's overall harmonic distortion is low—0.01% or less at 3-Vrms output into a 500-Ω load with no overall feedback. Even with no overall feedback, the circuit's response to a ±5-V, 10-kHz square wave input, band limited to 1 μs, has no overshoot. If needed, setting bias resistor R_B lower can accommodate even steeper input-signal slopes and drive lower impedance loads with high linearity. The main trade-off for both objectives is more power dissipation. A secondary trade-off is the need for retrimming the source-bias resistor R_2.□